EXHIBIT L

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00711
Patent No. 10,860,506

PATENT OWNER RESPONSE

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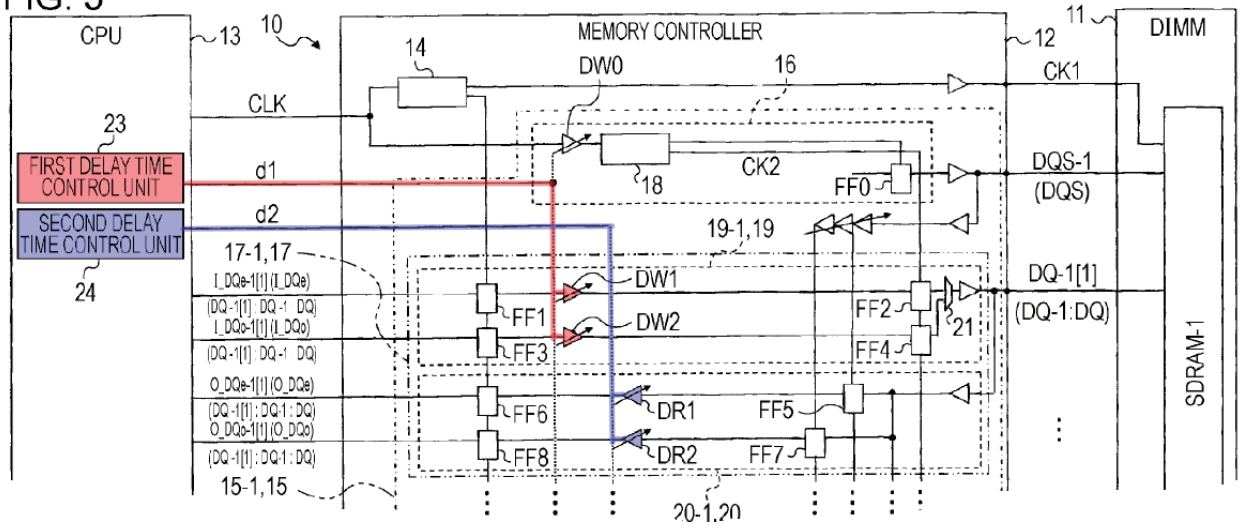
signals and clock signal from the system memory controller will arrive at respective SDRAMs on the memory module at substantially the same time. EX1006, 2:39-45, 12:59-63; E2006, ¶68. These delays are determined by, and carried out under the control of, a first delay time control unit 23 (highlighted in red below) and second delay time control unit 24 (highlighted in blue below) ***located in the computer's CPU 13***. *See e.g.,* EX1006, FIGs. 4-6, 8, 9, 12-15. The CPU's first and second delay time control units 23 and 24 output control signals on dedicated control signal lines d1 and d2 to control variable delay circuits DW and DR in the memory controller 12. See annotated partial reproduction of FIG. 5 from Tokuhiro below.

FIG. 5



Tokuhiro explains that the "first delay time control unit 23 outputs the respective first control signals d1 to the first variable delay circuits DW-1 to DW-n so that the set first delay times Dt1-1 to Dt1-n are obtained." *Id.*, 14:59-62. Moreover, "[t]he second delay time control unit 24 controls the second variable

delay circuit DR … to delay the data signal by the second delay time Dt2 … and it outputs the second control signal d2 for setting the second delay time Dt2." *Id*., 15:3-9; EX2006, ¶¶69-70.

VIII. THE PETITIONER FAILED TO ESTABLISH THAT ANY CLAIM OF THE '506 PATENT IS UNPATENTABLE UNDER GROUND 1

Ground 1 relies on Hiraishi alone, or alternatively in combination with Butt. In either case, the Petition is facially deficient and does not establish that any claim of the '506 patent is unpatentable.

A. Hiraishi Does Not Disclose Delaying a Read Strobe Based on Signals Received by the Data Buffer During a Previous Operation

1. Hiraishi's Delay Circuit Applies Only a Fixed Delay

Petitioner has failed to show that Hiraishi discloses a "first data buffer … configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe," where "the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations," as required by independent claim 1 (referred to herein as the "strobe delay feature"). The same deficiency exists for independent claim 14.[2]

[2] Claims 15-17 depend, either directly or indirectly, on independent claim 14 and further recite a predetermined amounts of delay "determined based on signals received by the second data buffer during one or more previous operations."

Petitioner relies on the strobe signal output by Hiraishi's delay circuit 372 as being the claimed "first delayed read strobe" and Hiraishi's delay of "about 90 degrees" as being the claimed "first predetermined amount" of delay. *See* Pet., 35. Petitioner contend that Hiraishi's S4 read leveling and read leveling circuit 323 apply fine timing delays adjustments to the DQS signals. *See* Pet., 40. Petitioner's arguments fail for multiple reasons.

First, Hiraishi's S4 read leveling is used to time the internal signal that turns on input buffers INB; it is not used to adjust the delay of the read strobe signal caused by the delay circuit 372. *See* EX1005, FIG. 5, FIG. 15, [0028], [0147-0151] ("The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, ***and used in an adjustment of an activation timing of the input buffer circuit INB and the like***.");[3] *supra*, § VII.A.2; EX2006, ¶¶73-74. Dr. Wedig agreed that the read leveling in Hiraishi adjusts the timing of the activation of input buffers INB. EX2008, 59:4-18.[4] Because of flight

[3] Emphasis added throughout unless otherwise indicated.

[4] While Dr. Wedig suggests that the phrase "and the like" implies Hiraishi performs additional read leveling functions, he admitted that "it's not given in any more detail than that …." EX2008, 59:19-60:18. In fact, a POSITA would

time delays, the read data might arrive at one data register buffer at a later time than the corresponding data would arrive at a second data register buffer on the same module. EX1005, FIG. 15; EX2006, ¶75. Accordingly, the purpose of Hiraishi's read leveling circuit 323 is to allow the data register buffers 300 to turn on their INB input buffers connected to the L1 and L2 buses in time for them to receive the incoming data from the memory chips 200. *See id*.; EX1005, [0151]; EX2008, 59:4-18 (Dr. Wedig describing Hiraishi's adjustment of the "activation timing of the input buffer" as "determin[ing] when to activate it, when to enable it, when to turn it on … [s]o it allows the data to pass when it's activated."). As such, Hiraishi simply describes read leveling that adjusts the timing of when the input buffers INB are turned on so they are active when data arrives. EX2006, ¶¶58-60; *see supra*, § VII.A.2.

Second, Hiraishi describes delaying the DQS signal by a fixed 90 degrees (1/4 clock cycle) by delay circuit 372, relative to the input DQS 351 or 352. EX1005, [0091]. There is no teaching or suggestion in Hiraishi that delay circuit 372 performs any "fine timing adjustments to the DQS signals by read leveling circuit 323," as Petitioner alleges. EX2006, ¶76. Nor can Petitioner point to any signal from the read

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understand "and the like" merely refers to related activation timing operations. EX2006, ¶59.

leveling circuit 323 that is inputted to the delay circuit 372 that could affect any such adjustment. *See infra*, Section VIII.A.2; EX2006, ¶77.

Hiraishi describes that this fixed "about" 90 degree delay is applied by delay circuit 372 in the case of a read operation. *See* EX1005, [0091]. However, the ***only*** input to delay circuit 372 described anywhere in Hiraishi is a DQS signal (either from L1 or L2 based on selector 332). *See* EX1005, [0091] ("[T]he selector 332 selects a data strobe signal DQS input from either one of the input/output terminals 351 and 352. A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal."). As Dr. Mangione-Smith explains, a POSITA would thus understand from Hiraishi's disclosure that the delay circuit 372 applies a fixed phase shift, and not a delay based on signals received by the buffer during a previous operation, as required by the strobe delay feature of the '506 patent. EX2006, ¶78.

That Hiraishi adds a fixed 90-degree delay is supported by both the express teachings of Hiraishi, as well as the DDR3 standard. For example, in describing FIG. 11, which is a timing chart for a read operation of memory module 100, Hiraishi states that "[t]he data register buffer 300 loads the read data DQ that is output from the memory chip 200 in the FIFO (Read) circuit 302 with a data strobe signal DQS that is delayed by a ***predetermined phase amount*** (for example, phase difference of

about 90 degrees). EX1005, [0129]. Moreover, a 90-degree delay (or quarter clock cycle) is the same fixed base delay added by Butt. EX1029, [0021]; EX2008, 76:24-77:2, 122:5-25. This is not a coincidence. Per the DDR standard, memory devices provide the data strobe edge-aligned with the data for read operations, and therefore it is necessary to shift the edges of the DQS signal about a quarter clock cycle toward the center of the data periods for read operations. EX2006, ¶79; *see supra*, Section III.

Third, Hiraishi has no need to vary the delay applied to the DQS strobe signal because the DQ read data and DQS strobe signal arrive at the data buffer already edge-aligned, despite Petitioner's suggestion otherwise. Hiraishi is very clear on this. Hiraishi's figures show that DQ read data and DQS strobe signal are aligned (as required by the DDR standard) as they are received from the memory devices. EX1005, FIG. 11, 15; EX2006, ¶80. For example, Hiraishi describes that "there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300." EX1005, [0129]. But this "flight time" is the same for both the read data DQ and the date strobe signal DQS, as shown in Hiraishi's FIG. 11, partially reproduced below, where the DQS(IN) and DQ(IN) have the same "Flight Time" and arrive at the data buffer edge-aligned. EX2006, ¶80.

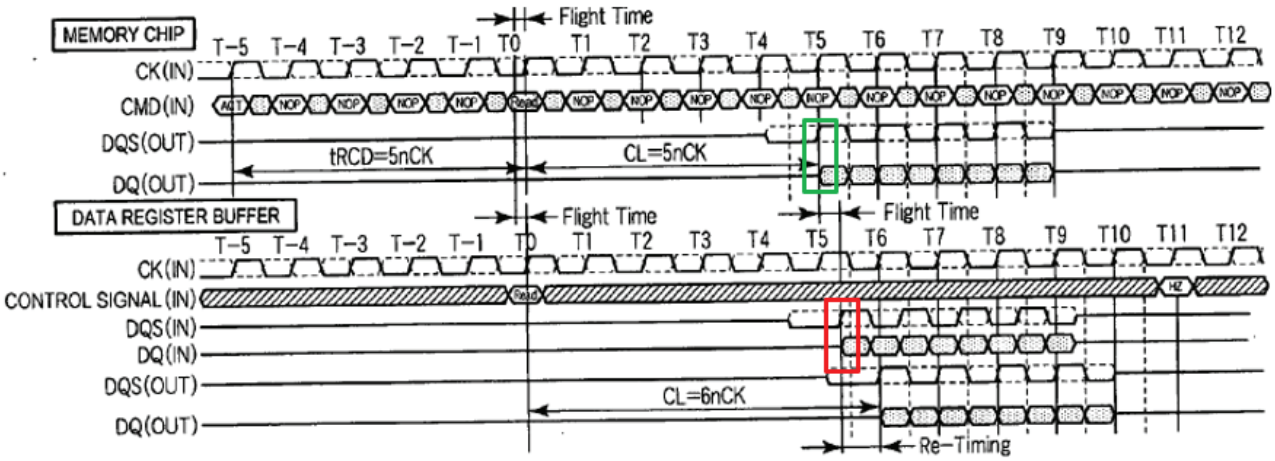

FIG.11

Similarly, Hiraishi shows in FIG. 15 that, while flight time varies as between different memory devices (*e.g.*, memory chip 200-0 and memory chip 200-19), the DQ data and DQS strobe received by the data buffer from any given memory device is always edge-aligned.

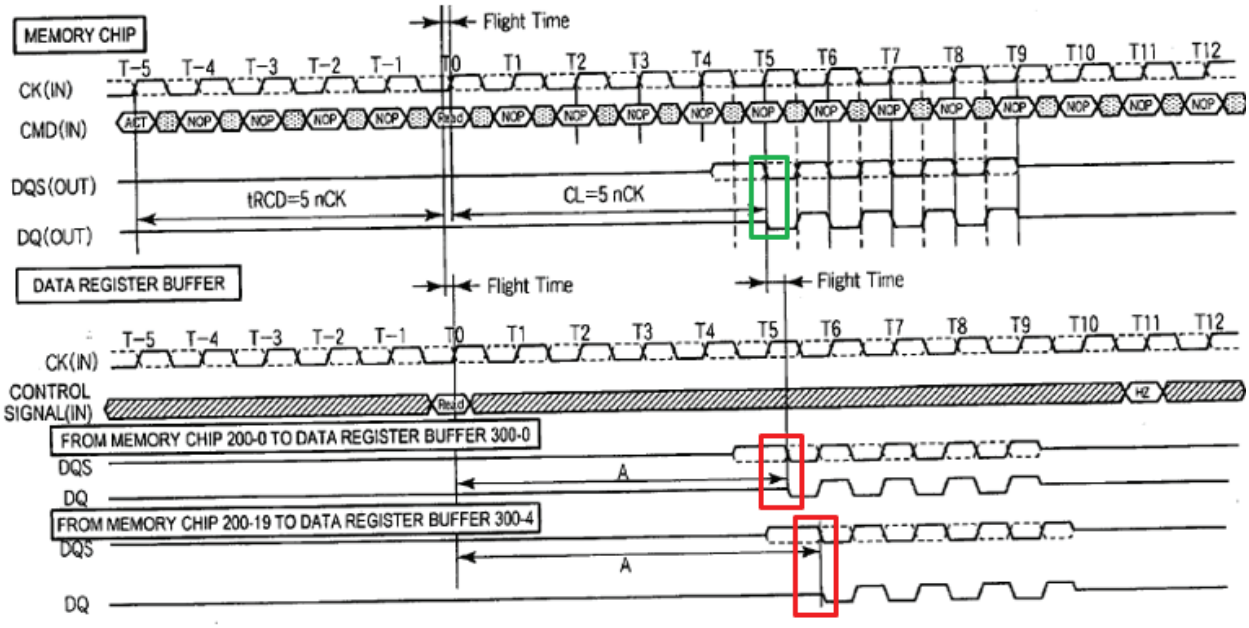

FIG.15

EX2006, ¶81.

As to Hiraishi's use of the term "about," this would be understood by a POSITA to simply follow from the fact that all electrical components inherently have operating tolerances, as Dr. Wedig acknowledges. EX2008, 95:8-96:1 (describing how "there's going to be various variables in temperature, process, voltage fluctuations, crosstalk, that could cause [timing] to not be perfect" and that this "applies to every component in every electronic system that I've ever worked with."). Therefore, a POSITA would understand that Hiraishi's reference to "***about*** 90 degrees" is meant to reflect no more than the imprecise nature of adding fixed amounts of delay to DQS signals, particularly over a range of operating speeds. EX2006, ¶82. Patent Owner's DDR DRAM patents show signal delays are often described as being "about" a given phase shift. EX2009 (US8055930), 11:58-67, 13:55-14:3.

2. Hiraishi's Read Leveling Circuit Does Not Control the Delay Circuit

The fact that Hiraishi delay circuit 372 does not apply a delay determined based on signals received during a previous operation is also clear from the fact that, contrary to Petitioner's contention, the read leveling circuit 323 does not control the delay circuit 372. EX2006, ¶ 84. Specifically, the data register control circuit 320 (which includes read leveling circuit 323) is neither physically nor functionality connected to the delay circuit 372. For example, FIG. 5 describes the data register control circuit 320 as providing only 4 outputs: (1) buffer control (BC) signals to the

various input buffers INB and output buffers OUTB buffers (highlighted in red), (2) a "select signal SEL" that controls operation of selectors 331-334 (highlighted in blue), (3) a feedback signal DRF supplied to the external command/address/control register buffer 400 ((highlighted in purple), and (4) a clock displacement signal provided to DLL circuit 310 (highlighted in green).

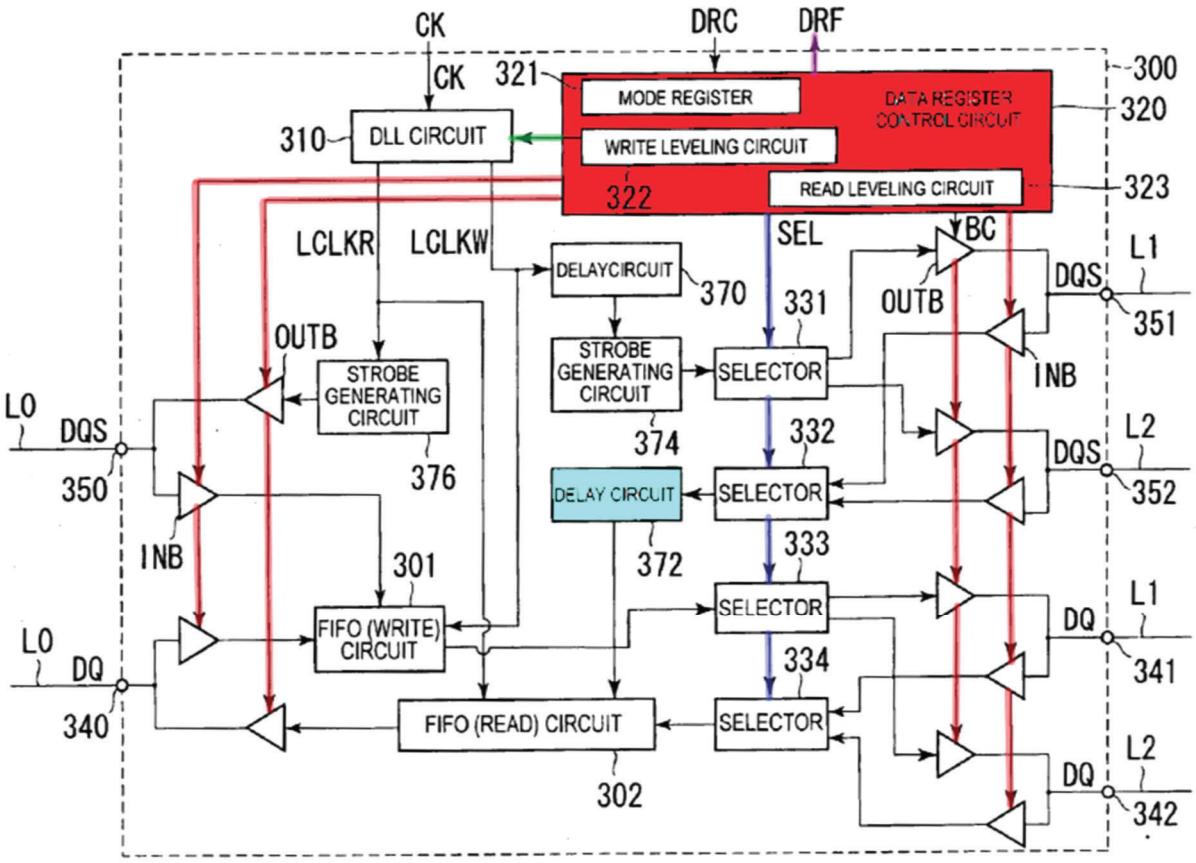

FIG.5

With respect to Output 1 (highlighted in red above), Hiraishi explains that the BC signals are provided to control the operation of the various input buffers INB and output buffers OUTB, none of which is the delay circuit 372. EX1005, [0088]; EX2006, ¶¶84-85. Dr. Wedig confirmed those are control signals for the input

buffers INB and output buffers OUTB. EX2008, 91:22-92:20. Specifically, a POSITA would understand that the BC signals provided to the INB buffers are for adjusting the timing of when the input buffers INB are turned on so they are active when data arrives. *See supra*, §§ VII.A.2, VIII.A.1; EX2008, 59:4-18; EX2006, ¶¶ 85-86.

With respect to Output 2 (highlighted in blue above), the "select signal SEL" is used to control operation of selectors 331-334, as Dr. Wedig confirmed (EX2008, 92:21-23), which select different input/output terminals for data (i.e., terminal 341 or 342) and for DQS strobe signals (terminal 351 or 352). EX1005, [0088], [0091]; EX2006, ¶87.

With respect to Output 3 ((highlighted in purple above), the feedback signal DRF is supplied to the external command/address/control register buffer 400 and is used to indicate a current status of the data register buffer 300. EX1005, [0089]; EX2006, ¶88; EX2008, 97:23-98:8. Petitioner does not rely on DRF for performing the alleged fine adjustment.

With respect to Output 4 ((highlighted in green above), the clock displacement signal provided to DLL circuit 310, which generates internal clock signals LCLKR and LCLKW based on the CK signal entering the buffer 300. EX2006, ¶89; EX2008, 93:3-94:5. As the paths highlighted in green below show, the DLL circuit 310

generates local clock signal LCLKR that is used by the strobe generating circuit 376 to generate DQS on terminal 350. EX2006, ¶89; EX2008, 93:24-94:5.

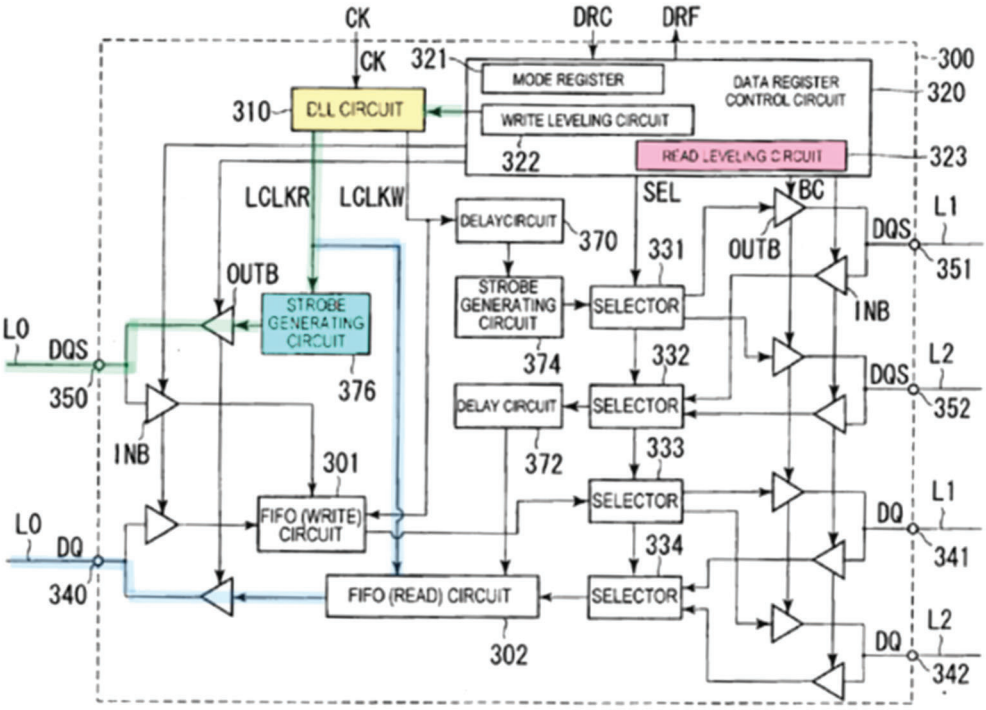

FIG.5

Moreover, as highlighted in blue above, "[a]n output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310." EX1005, [0087]. The LCLKR, however, is not an input to delay circuit 372, nor can it otherwise affect the delay applied by circuit 372. EX2006, ¶90. Similarly, the DLL circuit 310 generates the local clock signal LCLKW, which is used by the strobe generating circuit 374 to generate new DQS signals on terminal 351 or 352, and which is in sync with the clock in the memory devices, as Dr. Wedig confirmed. EX2008, 93:11-23; *see supra*, Section VII.A.2.

The path for the strobe generated by circuit 374 and transmitted to terminal 351/352 relates to the write operations and not the read operations at issue here. EX1005, [0091]; EX2006, ¶91. Petitioner does not assert that circuits 370 or 374 affects the output by delay circuit 372.

In short, the delay applied by Hiraishi's delay circuit 372 is fixed and is not controllable by the data register control circuit 320, and Hiraishi does not disclose any other control circuit in data buffer 300, as Dr. Wedig confirmed. EX2008, 100:6-20; EX2006, ¶¶84-92. Moreover, Petitioner has not proposed any modifications to Hiraishi's circuitry. EX2008, 139:9-140:8. As such, the Petitioner has failed to show that Hiraishi teaches or suggests the strobe delay feature—specifically that "the first predetermined amount [of delay to the read strobe] is determined based at least on signals received by the first data buffer during one or more previous operations," as recited in claim 1 and reflected in the limitations of claim 14.[5]

[5] The Petitioner does not advance different arguments for the strobe delay feature of independent claim 14 (*see* Petition, 64), or suggest there are any material differences between claims 1 and 14. *See* Petition, 61-64.

B. The Petitioner Has Failed to Establish that a POSITA Would Have Had a Reasonable Expectation of Success in Achieving the Claimed Invention

Recognizing that Hiraishi does not disclose the strobe delay feature, Petitioner alternatively looks to Butt in search of the missing limitation. *See* Petition, 44-48. However, Petitioner's attempt to retrofit Hiraishi with the missing limitation fails to include a showing that a POSITA would have had a reasonable expectation of achieving the strobe delay feature when combining Hiraishi and Butt, as proposed.

At institution, the Board credited Dr. Wedig's testimony that a person of ordinary skill would have had a reasonable expectation of success ***in making the combination***." Paper 14, 22-23 (citing EX1003, ¶149 (Dr. Wedig testifying that "a Skilled Artisan would have had a reasonable expectation of success in ***making such a combination***."). However, respectfully, that is not the correct inquiry. *See Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) ("The Board seemed to believe that the 'reasonable expectation of success' inquiry looked to whether one would reasonably expect the prior art references to operate as those references intended once combined. That is not the correct inquiry—one must have a motivation to combine accompanied by a reasonable expectation of ***achieving what is claimed***.").

Petitioner's proclamation that a POSITA would have had a reasonable expectation of success is supported only by Dr. Wedig's testimony that "application

XI. CONCLUSION

The Board should find all claims of the '506 patent are not unpatentable.

Dated: January 31, 2023

Respectfully submitted,

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